

DIALOG(R)File 347:JAPIO

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02830934 **Image available**

MOUNTING METHOD FOR SEMICONDUCTOR ELEMENT ON TRANSPARENT
SUBSTRATE

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ABSTRACT

PURPOSE: To shield a light at an IC chip simultaneously during the manufacture of a semiconductor element and to further reduce the stray capacitance due to wirings by forming a light shielding film during manufacturing step of a FET, shielding a light incident from a glass substrate, and setting a distance between a conductive material and the film to a specific value or less.

CONSTITUTION: A light shielding gate electrode 2 is formed of Cr on a glass substrate 1. A light shielding layer 3 of a COG region is held at a ground potential or a predetermined potential. The height 50 of bump for connecting an IC chip 1 to a wiring conductive film 9 by a COG bump 10 is so set that the distance between a wiring conductive film 9 and the chip 11 becomes $1\mu\text{m}$ or more. This is because, if a dust is engaged, it might be short-circuited. Further, this is because, when the height 50 of the bump is set $10\mu\text{m}$ or more, the forming accuracy of the bump itself is deteriorated. In order to complete as a liquid crystal display, an opposite glass substrate containing a color filter, opposite electrode, etc., is disposed on a TFT region isolated at 1mm or more from the chip 11.

DIALOG(R)File 352:DERWENT WPI
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007924112 **Image available**

WPI Acc No: 89-189224/198926

Semiconductor device mounted onto transparent substrate - has thin film
split transistor layer transparent gate electrode, thin insulating layer
and also drain and source NoAbstract Dwg 4/4

Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
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Priority Applications (No Type Date): JP 87287880 A 19871113

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
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Title Terms: SEMICONDUCTOR; DEVICE; MOUNT; TRANSPARENT; SUBSTRATE;
THIN;

FILM; SPLIT; TRANSISTOR; LAYER; TRANSPARENT; GATE; ELECTRODE; THIN;
INSULATE; LAYER; DRAIN; SOURCE; NOABSTRACT

Derwent Class: U11; U12; U14

International Patent Class (Additional): H01L-021/60; H01L-027/12

File Segment: EPI